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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/253,995	02/22/1999	YOSHIHIRO SAGA	B208-1021	6335

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EXAMINER
HANNETT, JAMES M

ART UNIT	PAPER NUMBER
2612	8

DATE MAILED: 06/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/253,995	SAGA, YOSHIHIRO	
	Examiner	Art Unit	
	James M Hannett	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *41-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *41-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 41-50 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1: Claims 41-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 5,146,592 Pfeiffer et al.

2: As for Claim 41, Pfeiffer et al teaches in Figure 1 the use of an image processing apparatus comprising: an image capture unit adapted (10) to capture image data, Column 5, Lines 58-66. Pfeiffer et al teaches that the image processing apparatus has storage means for storing image data. Pfeiffer et al teaches on Column 22, Lines 33-40 that the image processing apparatus has a video DRAM refresh controller having a number of programmable registers for defining the various timing constraints and operations of the controller. Pfeiffer et al teaches on Column 23, Lines 20-34 that the image processing apparatus is capable of performing a first process of screen refresh and a second process of the image algorithm processor and states that both processes can access the image memory. Pfeiffer et al teaches on Column 23, Lines 24-32 that an arbitration circuit is provided to determine the priority of the various requests to access memory. Pfeiffer et al teaches that the screen refresh function of the video DRAM shift registers is given top

priority (which is viewed as the process of storing the image data), followed by refresh of the DRAM cells, and then address request from the image algorithm processor.

Pfeiffer et al teaches on Column 9, Lines 7-23 that the image algorithm processor carries out substantially all of the image and graphics address computations for providing data to the image computer. Pfeiffer et al teaches that the image algorithm processor is the master controller of the image computer, providing addresses for the image memory and thus data for the parallel image processor set in carrying out data processing tasks.

Official notice is taken that it was commonly know in the art at the time the invention was made to include compression and expansion abilities in a digital camera which was commonly performed by the image processor in order to allow image data to be stored in a smaller required memory size.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include compression and expansions capabilities in the image processor in order to allow the image data to be stored in a reduced memory size.

Pfeiffer et al further teaches on Column 9, Lines 7-23 that the image algorithm processor carries out substantially all of the image and graphics address computations for providing data to the image computer. Pfeiffer et al teaches that the image algorithm processor is the master controller of the image computer, providing addresses for the image memory and thus data for the parallel image processor set in carrying out data processing tasks.

3: In regards to Claim 42, Pfeiffer et al teaches the refresh control unit is also adapted to assign a higher priority to a process of displaying the image data stored in the memory than the process of refreshing the memory. Pfeiffer et al teaches on Column 21

and 22, Lines 67-68 and 1-13 that the screen refresh controller enables serial shift registers of the video DRAMs to be sequentially loaded and shifted in a timely manner to provide raster scan pixel data for a monitor. Pfeiffer et al teaches on Column 26, Lines 56-68 that the arbitration means performs a refresh request during the horizontal blanking period of the image data being displayed on the monitor.

4: As for Claim 43, Pfeiffer et al teaches that the image processing system includes an image capture unit (10) adapted to capture image data, Therefore, The system as taught buy Pfeiffer et al is viewed as a digital camera.

5: In regards to Claim 44, Pfeiffer et al teaches in Figure 1 the use of an image processing apparatus comprising: an image capture unit adapted (10) to capture image data, Column 5, Lines 58-66. Pfeiffer et al teaches that the image processing apparatus has storage means for storing image data. Pfeiffer et al teaches on Column 22, Lines 33-40 that the image processing apparatus has a video DRAM refresh controller having a number of programmable registers for defining the various timing constraints and operations of the controller. Pfeiffer et al teaches on Column 23, Lines 20-34 that the image processing apparatus is capable of performing a first process of screen refresh and a second process of the image algorithm processor and states that both processes can access the image memory. Pfeiffer et al teaches on Column 23, Lines 24-32 that an arbitration circuit is provided to determine the priority of the various requests to access memory. Pfeiffer et al teaches that the screen refresh function of the video DRAM shift registers is given top priority (which is viewed as the process of storing the image data), followed by refresh of the DRAM cells, and then address request from the image algorithm processor.

Pfeiffer et al teaches on Column 9, Lines 7-23 that the image algorithm processor carries out substantially all of the image and graphics address computations for providing data to the image computer. Pfeiffer et al teaches that the image algorithm processor is the master controller of the image computer, providing addresses for the image memory and thus data for the parallel image processor set in carrying out data processing tasks.

Official notice is taken that it was commonly know in the art at the time the invention was made to include compression and expansion abilities in a digital camera which was commonly performed by the image processor in order to allow image data to be stored in a smaller required memory size.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include compression and expansions capabilities in the image processor in order to allow the image data to be stored in a reduced memory size.

Pfeiffer et al further teaches on Column 9, Lines 7-23 that the image algorithm processor carries out substantially all of the image and graphics address computations for providing data to the image computer. Pfeiffer et al teaches that the image algorithm processor is the master controller of the image computer, providing addresses for the image memory and thus data for the parallel image processor set in carrying out data processing tasks.

6: As for Claim 45, Pfeiffer et al teaches the refresh control unit is also adapted to assign a higher priority to a process of displaying the image data stored in the memory than the process of refreshing the memory. Pfeiffer et al teaches on Column 21 and 22, Lines 67-68 and 1-13 that the screen refresh controller enables serial shift registers of the video DRAMs to be sequentially loaded and shifted in a timely manner to provide raster

scan pixel data for a monitor. Pfeiffer et al teaches on Column 26, Lines 56-68 that the arbitration means performs a refresh request during the horizontal blanking period of the image data being displayed on the monitor.

7: In regards to Claim 46, Pfeiffer et al teaches that the image processing system includes an image capture unit (10) adapted to capture image data, Therefore, The system as taught buy Pfeiffer et al is viewed as a digital camera.

8: As for Claim 47, Pfeiffer et al teaches in Figure 1 the use of an image processing apparatus comprising: an image capture unit adapted (10) to capture image data, Column 5, Lines 58-66. Pfeiffer et al teaches that the image processing apparatus has storage means for storing image data. Pfeiffer et al teaches on Column 22, Lines 33-40 that the image processing apparatus has a video DRAM refresh controller having a number of programmable registers for defining the various timing constraints and operations of the controller. Pfeiffer et al teaches on Column 23, Lines 20-34 that the image processing apparatus is capable of performing a first process of screen refresh and a second process of the image algorithm processor and states that both processes can access the image memory. Pfeiffer et al teaches on Column 23, Lines 24-32 that an arbitration circuit is provided to determine the priority of the various requests to access memory. Pfeiffer et al teaches that the screen refresh function of the video DRAM shift registers is given top priority (which is viewed as the process of storing the image data), followed by refresh of the DRAM cells, and then address request from the image algorithm processor.

Pfeiffer et al teaches on Column 9, Lines 7-23 that the image algorithm processor carries out substantially all of the image and graphics address computations for providing data to the image computer. Pfeiffer et al teaches that the image algorithm processor is

the master controller of the image computer, providing addresses for the image memory and thus data for the parallel image processor set in carrying out data processing tasks.

Official notice is taken that it was commonly know in the art at the time the invention was made to include compression and expansion abilities in a digital camera which was commonly performed by the image processor in order to allow image data to be stored in a smaller required memory size.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include compression and expansions capabilities in the image processor in order to allow the image data to be stored in a reduced memory size.

Pfeiffer et al further teaches on Column 9, Lines 7-23 that the image algorithm processor carries out substantially all of the image and graphics address computations for providing data to the image computer. Pfeiffer et al teaches that the image algorithm processor is the master controller of the image computer, providing addresses for the image memory and thus data for the parallel image processor set in carrying out data processing tasks.

9: In regards to Claim 48, Pfeiffer et al teaches the refresh control unit is also adapted to assign a higher priority to a process of displaying the image data stored in the memory than the process of refreshing the memory. Pfeiffer et al teaches on Column 21 and 22, Lines 67-68 and 1-13 that the screen refresh controller enables serial shift registers of the video DRAMs to be sequentially loaded and shifted in a timely manner to provide raster scan pixel data for a monitor. Pfeiffer et al teaches on Column 26, Lines 56-68 that the arbitration means performs a refresh request during the horizontal blanking period of the image data being displayed on the monitor.

10: As for Claim 49, The compression and expansion capabilities as discussed in Claim 47 are viewed as the process of processing the image data by changing a size of the image data.

11: In regards to Claim 50, Pfeiffer et al teaches that the image processing system includes an image capture unit (10) adapted to capture image data, Therefore, The system as taught buy Pfeiffer et al is viewed as a digital camera.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M Hannett whose telephone number is 703-305-7880. The examiner can normally be reached on 8:00 am to 5:00 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on 703-305-4929. The fax phone numbers for

the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-842-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to customer service whose telephone number is 703-308-6789.

James Hannett
Examiner
Art Unit 2612

JMH
June 2, 2003

WENDY R. GARBER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600